PARTITIONING

PARTITIONING

- Efficient designing of any complex system necessitates decomposition of the same into a set of smaller subsystems. Subsequently, each subsystem can be designed **independently and simultaneously** to speed up the design process. The **process of decomposition is called partitioning.**
- Three broad parameters for efficiency of partitioning:
  - **original functionality** of the system remains **intact**.
  - an **interface specification** is generated during the decomposition, which is used to connect all the subsystems. The system decomposition should **ensure minimization of the interface interconnections** between any two subsystems.
  - the decomposition **process should be simple and efficient** so that the time required for the decomposition is a **small fraction of the total design time.**
-

PARTITIONING

- **Further** partitioning may be required in the events **where the size of a subsystem remains too large to be designed efficiently**. Thus, partitioning can be used in a **hierarchical manner until each subsystem created has a manageable size**.

PARTITIONING

- A computer system is comprised of tens of millions of transistors. It is partitioned into **several smaller modules/blocks** for facilitation of the design process.
- Each **block has terminals located at the periphery** that are **used to connect the blocks**.

PARTITIONING

- The connection is **specified by a netlist**, which is **a collection of nets**.
- A net is a **set of terminals which have to be made electrically equivalent.**

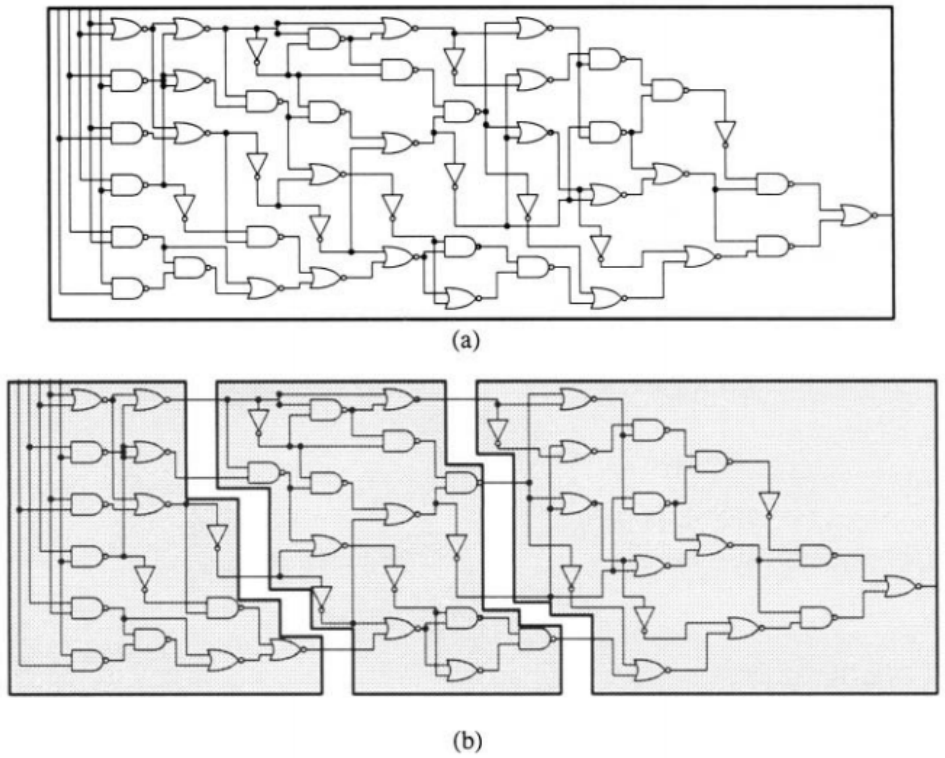

Figure 5.1: Partitioning of a circuit.

LEVEL OF PARTITIONING

- A VLSI system is **partitioned at several levels** due to its complexity. At the **highest** level, it is partitioned into a set of **sub-systems whereby each subsystem can be designed and fabricated independently on a single PCB.**

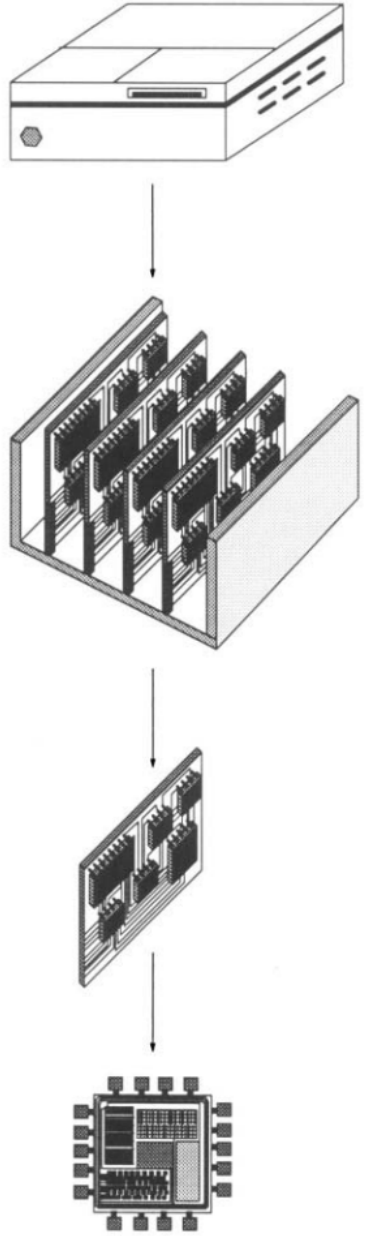

Figure 5.2: System hierarchy.

LEVEL OF PARTITIONING

- If the **circuit assigned to a PCB remains too large** to be fabricated as a single unit, it is further partitioned into subcircuits such that **each subcircuit can be fabricated as a VLSI chip**.
- Normally three levels:
  - The partitioning of a **system into a group of PCBs** is called the **system level** partitioning.
  - The partitioning of a **PCB into chips** is called the **board level** partitioning.
  - The partitioning of a **chip into smaller subcircuits** is called the **chip level** partitioning.

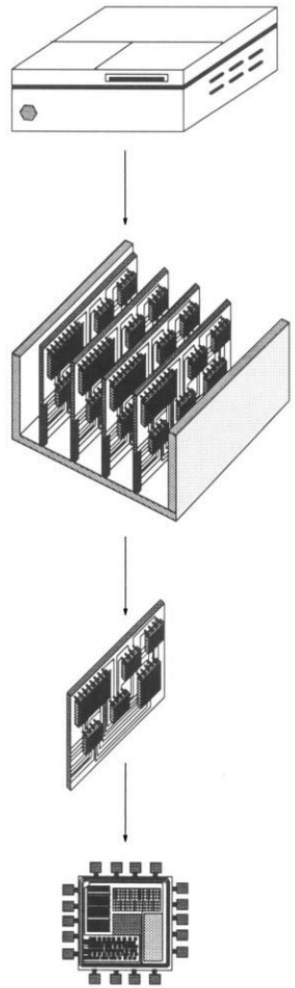

Figure 5.2: System hierarchy.

SYSTEM LEVEL PARTITIONING

- Each PCB usually has a **fixed area**, and a **fixed number of terminals** to **connect with other boards**. The number of **terminals available** in one board (component) to **connect** to other boards (components) is called **the terminal count** of the board (component).
- The **reliability** of the system is **inversely proportional to the number of boards** in the system.
  - one of the objectives of partitioning is to **minimize the number of boards**. Another important objective is the **optimization of the system performance**. Partitioning must **minimize any degradation of the performance** caused by the **delay due to the connections between components** on different boards.
  - The **signal carried by a net** that is **cut by partitioning** at this level has to **travel from one board to another board through the system bus.**
  - The **system bus is very slow** as the bus has to adhere to some **strict specifications** so that a variety of different boards can share the same bus.
- The **delay** caused by **signals traveling between PCBs** (off-board delay) plays a major role in determining the **system performance** as this delay is much **larger than the on-board** or the **on-chip delay**.

BOARD LEVEL PARTITIONING

- Unlike boards, **chips can have different sizes and can accommodate different number of terminals.**
  - The **terminal count** of a chip depends on the **package of the chip**. A Dual In-line Package (DIP) allows only 64 pins while a Pin Grid Array (PGA) package may allow as many as 300 pins.
- It is expedient that the **number of chips** used for each board be **minimized for enhanced board reliability.**
- **Minimization of the number of chips** is another important determinant of **performance** because the **off-chip delay is much larger than the on-chip delay**.
  - This differential in delay arises because the **distance between two adjacent transistors on a chip is a few *um* while the distance between two adjacent chips is in *mm***.
  - the signal has to travel between **chips, and through the connector**.
  - **connector** used to attach the chip to the board **typically has a high resistance and contributes significantly** to the signal delay.

CHIP LEVEL PARTITIONING

- The circuit assigned to a chip can be **fabricated as a single unit.**
- A chip can accommodate as many as **three million or more transistors**. The fundamental objective of chip level partitioning is to **facilitate efficient design of the chip.**
- After partitioning, **each subcircuit**, which is also called a **block**, can be **designed independently using either full custom or standard cell design style**.
- The **terminal count** for a partition is given by the **ratio of the perimeter of the partition to the terminal pitch.**
  - The **minimum spacing between two adjacent terminals is called terminal pitch** and is determined by the design rules.
  - The **number of nets which connect a partition to other partitions cannot be greater than the terminal count of the partition.**
  - In addition, the **number of nets cut by partitioning should be minimized** to **simplify the routing** task. The minimization of the number of nets cut by partitioning is one of the most important objectives in partitioning.

DISADVANTAGE!!

- A **disadvantage** of the partitioning process is that it may **degrade the performance** of the final design.
- Figure 5.4(a) shows two components A and B which are **critical to the chip performance**, and therefore, **must be placed close together**. However, due to partitioning, components A and B may be assigned to different partitions and may appear in the final layout as shown in Figure 5.4(b).

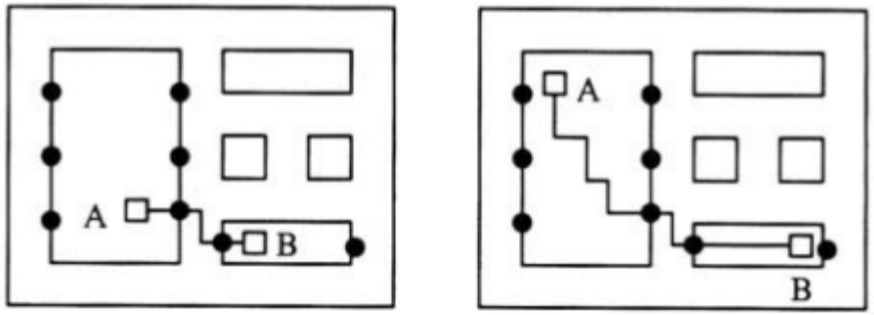

Figure 5.4: Bad partitioning increases the delay of circuit.

DISADVANTAGE!!

- The connection between A and B is very long, leading to a **very large delay and degraded performance.**
  - Thus, during partitioning, these **critical components** should be assigned to the **same partition**.
  - If such an assignment is **not possible**, then **appropriate timing constraints** must be generated to keep the **two critical components close together**.
- Chip performance is determined by **several components forming a critical path**.
- Assignment of these **components to different partitions extends the length of the critical path**. Thus, a major challenge for improvement of system performance is **minimization of the length of critical path**.

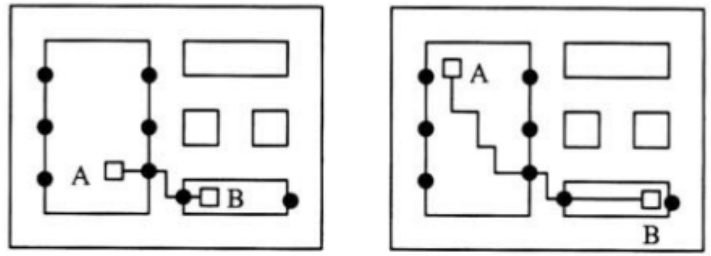

Figure 5.4: Bad partitioning increases the delay of circuit.

REFERENCE

- Sherwani
  - 5.1

ROUTING

- In the placement phase, the **exact locations** of circuit blocks and pins are **determined**.
- A **netlist** is also generated which **specifies the required interconnections.**
- **Space not occupied** by the blocks can be viewed as a **collection of regions**.
  - These regions are **used for routing** and are called as **routing regions**.

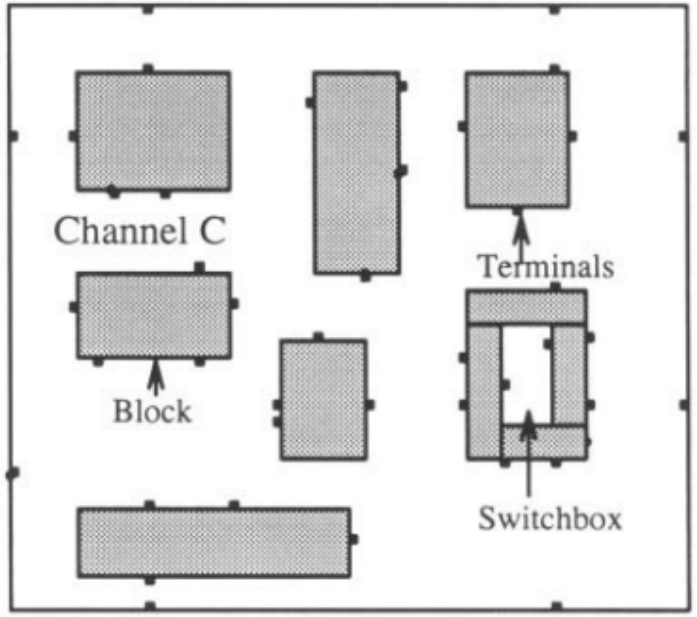

Figure 8.1: Layout of circuit blocks and pins after placement.

ROUTING

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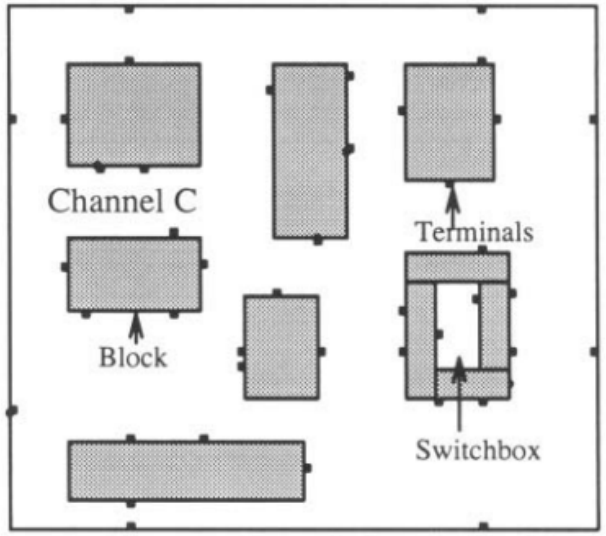

Figure 8.1: Layout of circuit blocks and pins after placement.